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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 09/905,195 | 07/16/2001 | Nobuaki Shinmori | KAN 135 | 3051 |
| 23995 | 7590 | 11/05/2004 | EXAMINER | |
| RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005 | | | DAMIANO, ANNE L | |
| | | ART UNIT | PAPER NUMBER | |
| | | 2114 | | |

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|------------------------|---------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 09/905,195 | SHINMORI | |
| | Examiner | Art Unit | |
| | Anne L Damiano | 2114 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 09 August 2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-8 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1 and 4-8 is/are rejected.
- 7) Claim(s) 2 and 3 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 09 August 2004 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All. b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Drawings

1. The drawings were received on 8/9/04. These drawings are acceptable.

Allowable Subject Matter

2. Claims 2 and 3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 4, recites the limitation "the date stored in the memory device" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim.

Claims 5-7 which are dependent on claim 4 are therefore also rejected.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwata et al. (6,662,314).

As in claim 1, Iwata discloses a semiconductor circuit comprising:

A JTAG (Joint Test Action Group Port) (*interface terminals-figure 2: component 11*);

A flash ROM that stores a security bit (*flash protect signal-must be stored*) (*figure 1: component 5 and column 4: line 64 column 5: line 6*);

A TAP (Test Access Port) that communicates with the flash ROM (*figure 2 components 15 and column 5: lines 63-column 6: lines 3, column 8: lines 29-33*) (*Controlling access to the data, is communication with the data-the flash ROM.*) and;

A JTAG control circuit (*figure 2: component 15*) controlled by the security bit of the flash ROM, the JTAG control circuit being connected between the JTAG port and the TAP (*The JTAG port and TAP are encompassed in the JTAG controller. Therefore, the JTAG control circuit is between the JTAG port and the TAP.*) and allowing or preventing communication of signals between the JTAG port and the TAP depending on the state of the security bit (*column 4:*

line 64-column 5: line 14) (If the rewriting of the internal flash is permitted, communication of signals between the JTAG port and the TAP is allowed. If the rewriting is prohibited, communication between the two is prevented.)

As in claim 8, Iwata discloses a semiconductor circuit comprising:

A memory device to store a control program and data (*program for rewriting data and internal flash information*) (*column 1: lines 60-64*);

A central processing unit to execute a specific process according to the program (*column 2: lines 41-46 and column 6: lines 5-24*);

A test port to input and output test signals (*JTAG interface terminals*) (*column 5: lines 63-66*);

A switch to control on/off between the test port and the central processing unit (*column 1: line 64-column 2: line 5 and column 4: line 64-column 5: line 6*);

A memory device (*program for rewriting data and internal flash information*) (*column 1: lines 60-64*); and

A security releasing means for comparing data input via the test port with the data stored in the memory device and turning on the switch when the two data agree (*column 18: line 66-column 19: line 10*). (*The security means do not permit then permit operation meaning that some form of switch must be existent for the different modes to occur according to the outcome of the comparison.*).

Response to Arguments

6. Applicant's arguments filed 8/9/04 have been fully considered but they are not persuasive.

A JTAG control circuit is clearly disclosed by Iwata in component 15 of figure 2 or figure 5 and column 5: line 63-column 6: line 1). See claim rejection for further explanation.

Security releasing means are certainly suggested by Iwata in column 18: line 3-column 19: line 10. The security means not permitting operations then permitting operations surely implies some sort of switch is present in the system. See claim rejection for further detail.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Art Unit: 2114

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (571) 272-3658. The examiner can normally be reached on M-F 9-6:30 first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALD



SCOTT BADERMAN
PRIMARY EXAMINER